Notice of Allowability	Application No.	Applicant(s)	
	09/930,365	TAKEUCHI, MASAHIRO	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/28/06*.

2. ☒ The allowed claim(s) is/are *25,51-54,56,63-67 and 69*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☒ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *6/1/2006* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SHOUXIANG HU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Alan S. Raynes (RN: 39,809) on June 1, 2006.

The application has been amended as follows:

IN THE CLAIMS

1-24. (canceled)

25. (currently amended) A method as in claim ~~24~~63, wherein the thermally treating the dielectric layer is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen.

26-50. (canceled)

51. (currently amended) A method for manufacturing a semiconductor device having a trench isolation region according to claim ~~40~~63, wherein the trench includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer thereon, wherein the dielectric layer is formed in direct contact with the thermal oxide layer.

52. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 51, wherein the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700°C to 1150°C.

53. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 51, wherein the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of 950 to 1150°C.

54. (previously presented) A method for manufacturing a semiconductor device having a trench isolation region according to claim 51, wherein the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm.

55. (canceled)

56. (currently amended) A method for manufacturing a semiconductor device having a trench isolation region according to claim ~~40~~63, wherein the trench is formed with a trench width of no greater than 0.35 μm.

57-62. (canceled)

63. (currently amended) A method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor substrate having an epitaxial layer thereon;

forming a pad layer on the epitaxial layer;

forming a polishing stopper layer on the pad layer;

forming at least one trench by etching the epitaxial layer while using at least the polishing stopper layer as a mask;

forming a dielectric layer in and above the at least one trench;

planarizing the dielectric layer using the polishing stopper layer as a stopper;

etching the polishing stopper layer after planarizing the dielectric layer;

etching the pad layer and exposing the epitaxial layer, after the etching the polishing stopper layer;

forming a sacrificial oxide layer on the exposed epitaxial layer, wherein the sacrificial oxide layer consists of an oxide layer formed by thermally oxidizing the exposed epitaxial layer, after the removing the pad layer;

wherein the sacrificial oxide layer is not formed on the dielectric layer;

thermally treating the dielectric layer at a temperature of at least 1100°C after the forming the sacrificial oxide layer;

after the thermally treating the dielectric layer at a temperature of at least 1100°C, implanting impurity ions in the epitaxial layer; and

after the implanting impurity ions, removing the entire sacrificial oxide layer and an upper portion of the dielectric layer using isotropic etching.

64. (previously presented) A method according to claim 63, further comprising forming a thermal oxide layer in the at least one trench prior to the forming a dielectric layer in and above the at least one trench.

65. (previously presented) A method according to claim 63, wherein the dielectric layer is formed with a film density of at least $2.1 g/cm^3$.

66. (previously presented) A method according to claim 65, wherein the dielectric layer is formed by a high density plasma CVD method.

67. (previously presented) A method according to claim 63, wherein the epitaxial growth layer has a thickness of at least 2 μm.

68. (canceled)

69. (currently amended) A method as in claim ~~68~~63, wherein the thermally treating the dielectric layer is carried out at a temperature in the range of 1100-1250°C.

Allowable Subject Matter

Claims 25, 51-54, 56, 63-67 and 69 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SH
June 1, 2006

SHOUXIANG HU
PRIMARY EXAMINER